ELECTRONIC CIRCUITS II EE338K

INDEX

FEEDBACK TOPOLOGIES

AMPLIFIER TYPE	INPUT	FED BACK AS	OUTPUT	MONITORS	Z_{IN}	Z_{OUT}
VCVS Voltage controlled voltage source, inverting	parallel	current	parallel	voltage	0	0
VCVS Voltage controlled voltage source, non-invert.	series	voltage	parallel	voltage	∞	0
CCVS Current controlled voltage source	parallel	current	parallel	voltage	0	0
VCCS Voltage controlled current source	series	voltage	series	current	∞	∞
CCCS Current controlled current source	parallel	current	series	current	0	∞

Parallel input – input signal always goes into the negative input
Series input – input signal always goes into the positive input

MORE TERMINOLOGY

Gain margin is the number of decibels the loop gain magnitude is below 0 dB at the frequency of phase reversal. 10 dB is considered safe.

Phase margin is the number of degrees the loop gain phase change is short of phase reversal at the frequency at which the magnitude of the loop gain is unity. 45° or more is considered safe.

AMOUNT OF FEEDBACK

$$\text{feedback (dB)} = 20\log_{10}\frac{A}{A_f}$$

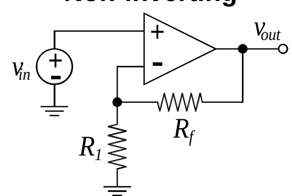
$$= 20\log_{10}|A| \quad - \quad 20\log_{10}|A_f|$$

= open loop gain [dB] – closed loop gain [dB]

FEEDBACK TOPOLOGIES

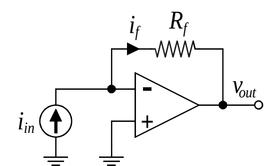
Four of the amplifier types described in more detail on the following page provide us with a complete set of the possible arrangements or **topologies** obtainable in a feedback system.

Non-inverting



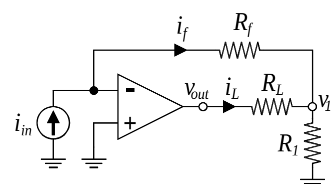
$$A_{f\infty} = \frac{v_{out}}{v_{in}} = \frac{R_1 + R_f}{R_1} \ \textbf{V/V}$$

Transresistance



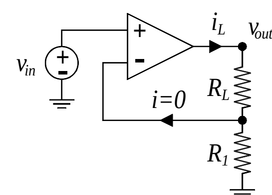
$$A_{f\infty} = \frac{v_{out}}{i_{in}} = -R_f \ \textbf{V/A}$$

Current



$$A_{f\infty} = \frac{i_L}{i_{in}} = -\frac{R_1 + R_f}{R_1} \ \textbf{A/A}$$

Transconductance



$$A_{f\infty} = \frac{i_L}{v_{in}} = \frac{1}{R_1} \ \textbf{A/V}$$

OP AMP FEEDBACK CIRCUITS

$A_{f\infty}$ denotes **asymptotic gain** and means voltage across the inputs and current into the inputs are zero, $A \to \infty$.

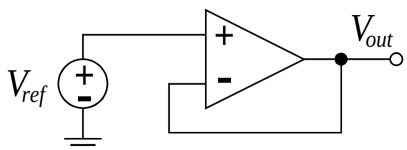
A_f denotes **closed loop gain**, called *finite A*, and takes into account the small voltage across the inputs $V_{out} = A(V_+ - V_-)$

A denotes **open loop gain** and is the op amp gain, typically about 10^5.

VOLTAGE FOLLOWER OR UNITY GAIN AMPLIFIER

$$V_{out} = A(V_+ - V_-)$$

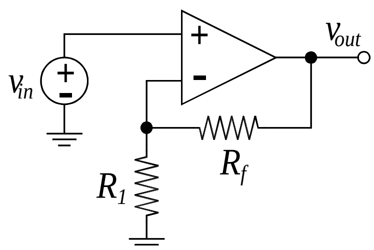
$$\frac{V_{out}}{A} = V_{ref} - V_{out}$$



If A is very large then $V_{out} = V_{ref}$

VCVS – NON-INVERTING VOLTAGE AMPLIFIER

provides an output voltage proportional to the input voltage. Series, hi-Z input; parallel, lo-Z out.



$$A_{f\infty} = \frac{v_{out}}{v_{in}} = \boxed{\frac{R_1 + R_f}{R_1}}$$

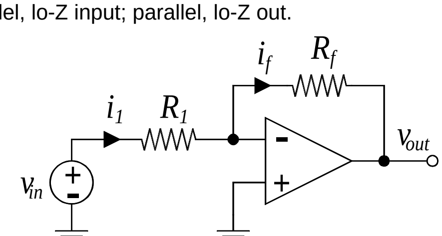
$$A_f = \frac{v_{out}}{v_{in}} = \frac{1}{\frac{1}{A} + \frac{R_1}{R_1 + R_f}} \qquad \boxed{\beta = \frac{R_1}{R_1 + R_f}}$$

We approach asymptotic conditions if $A >> \frac{R_1 + R_f}{R_1}$

VCVS - INVERTING VOLTAGE AMPLIFIER

Provides an output voltage that is proportional but of opposite polarity to the input voltage. Parallel, lo-Z input; parallel, lo-Z out.

$$\boxed{\beta = \frac{R_1}{R_1 + R_f}}$$



$$A_{f\infty} = \frac{v_{out}}{v_{in}} = \boxed{-\frac{R_f}{R_1}} \qquad A_f = \frac{v_{out}}{v_{in}} = \frac{-\frac{R_f}{R_1 + R_f}}{\frac{1}{A} + \frac{R_1}{R_1 + R_f}}$$

CCVS - TRANSRESISTANCE AMPLIFIER

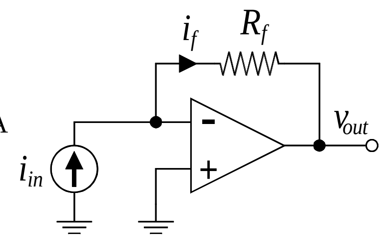
Current-controlled voltage source. The output voltage is proportional to the input current. Parallel, lo-Z input; parallel, lo-Z out.

$$i_{in} = i_f$$

$$v_{out} = -i_f R_f = -i_{in} R_f$$

$$A_{f\infty} = \frac{v_{out}}{i_{in}} = \boxed{-R_f} \text{ V/A}$$

$$z_{in} = R_{in} \parallel \left(\frac{R_f}{1 + A} \right)$$



z_{in} is typically less than 1 Ω

VCCS - TRANSCONDUCTANCE AMPLIFIER

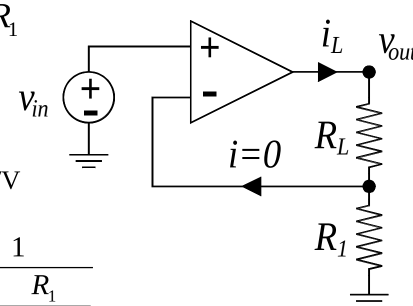
Voltage-controlled current source. The output current is proportional to the input voltage. Series, hi-Z input; series, lo-Z out.

$$v_{in} = v_+ = v_- = i_L R_1$$

$$i_L = \frac{v_{in}}{R_1}$$

$$A_{f\infty} = \frac{i_L}{v_{in}} = \boxed{\frac{1}{R_1}} \text{ A/V}$$

$$A_f = \frac{1}{R_1 + R_L} \times \frac{1}{\frac{1}{A} + \frac{R_1}{R_1 + R_L}}$$



We approach asymptotic conditions if $A >> \frac{R_1 + R_L}{R_1}$

CCCS - CURRENT AMPLIFIER

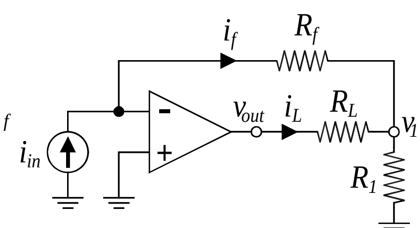
Provides a current output proportional to input current. Parallel, lo-Z input; series hi-Z output.

$$i_{in} = i_f$$

$$v_1 = -i_f R_f = -i_{in} R_f$$

$$v_1 = (i_f + i_L) R_1$$

$$= (i_{in} + i_L) R_1$$



$$A_{f\infty} = \frac{i_L}{i_{in}} = \boxed{-\frac{R_1 + R_f}{R_1}} \qquad A_f = -\frac{\frac{R_1 + R_f}{R_1} + \frac{1}{A}}{1 + \frac{1}{A}\left(1 + \frac{R_L}{R_1}\right)} \text{ A/A}$$

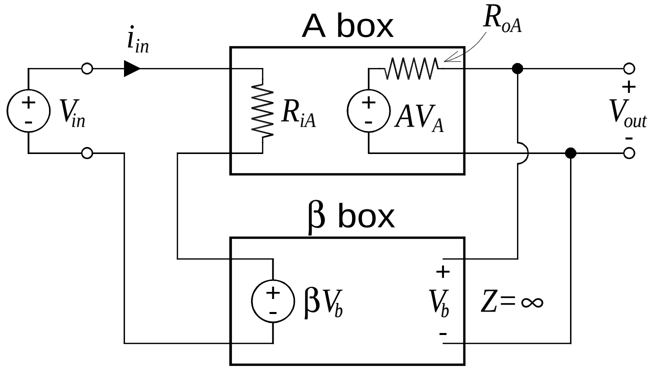
We approach asymptotic conditions if $A >> 1 + \frac{R_L}{R_1}$

GAIN ERROR

$$E\% \equiv \frac{\left(A_{f\infty} - A_f\right)}{A_{f\infty}} \times 100 = \frac{100}{1-L} \quad [\%]$$

A BOX - b BOX MODELING

The A box models the op amp and the b box models the feedback circuit as an ideal amplifier. The system shown models a non-inverting voltage-controlled voltage source topology (series input, parallel output), which is the most commonly used. This configuration is the basis for much discussion to follow.



$$A_f = \frac{v_{out}}{v_{in}} = \frac{A}{1+\beta A}$$

A_f = closed loop gain
A = open loop gain
β = feedback gain

D DESENSITIVITY FACTOR

feedback has the effect of *desensitizing* the gain of the system to changes in the A box gain (see *FEEDBACK AND GAIN*). Input and output impedance are also affected by a factor of D with the application of feedback. The desensitivity factor appears in many formulas as $1+\beta A$

$$D = 1+\beta A$$
$$= 1-L$$

A = open loop gain
β = b box gain
L = loop gain (a negative value)

b BETA and *L* LOOP GAIN

When the feedback circuit is thought of as a separate amplifier as shown in the A-box/β-box schematic, β is the ***gain*** of the feedback circuit. The value of β is normally less than one, and the small feedback signal is combined with the input signal 180° out of phase, which effectively reduces the gain of the amplifier (among other consequesces). L is called the **loop gain** and represents the amplifier gain once through the A-box/β-box loop. The value of L is always a negative number.

$$L = -b\,A$$
$$= 1-D$$

A = open loop gain or A box gain
β = b box gain
L = loop gain (a negative value)
D = desensitivity factor

FEEDBACK AND GAIN

The formula for closed loop gain of the A box - β box shown previously can be rewritten as follows:

$$A_f = \frac{v_{out}}{v_{in}} = \frac{1}{\frac{1}{A} + b}$$

With the value of A very large and the value of β somewhat less than one, the term $1/A$ will be much smaller than β. Therefore, with the use of feedback, the value of the gain A of the op amp (A box) now has little impact on the overall gain of the circuit.

FEEDBACK AND FREQUENCY RESPONSE

As shown below, feedback has the effect of extending the bandwidth by a factor of $1+\beta A$. However, since the gain is reduced by a factor of $1+\beta A$, the net result is that the gain bandwidth product remains constant, feedback or not.

$$A_f\,(j\omega) = \frac{1}{\frac{1}{A(j\omega)} + \beta}$$

Transfer function for an A box with one high frequency corner:

$$A(j\omega) = \frac{A_0}{1 + j\frac{f}{f_H}}$$

Adding feedback has the following effect:

$$A_{0f}\,(j\omega) = \frac{A_0}{1+\beta A_0}$$

$$f_{Hf} = \left(1+\beta A_0\right) f_H$$

$$f_{Lf} = \frac{f_L}{1+\beta A_0}$$

A_f (jω)= closed loop gain (sinusoidal steady state response)
A = open loop or A-box gain
A_0 = open loop passband gain
A_{0f} = closed loop gain in the passband
β = b box gain
f = frequency [Hz]
f_H = high corner frequency, the frequency at which the gain has dropped 3 dB below the passband gain without feedback [Hz]
f_{Hf} = high corner frequency, with feedback [Hz]
f_L = low corner frequency [Hz]
f_{Lf} = low corner frequency, with feedback [Hz]

FEEDBACK WITH MULTIPLE CORNER FREQUENCIES

Transfer function for an A box with n high frequency corners occurring at the same frequency:

$$A(j\omega) = \frac{A_0}{\left(1 + j\frac{f}{f_H}\right)^n}$$

with 1 low freq. corner:

$$A(j\omega) = \frac{A_0}{\left(1 - j\frac{f_L}{f}\right)}$$

Finding the **frequency of phase reversal** f_0 for the first function above:

$$-180° = -n\tan^{-1}\left(\frac{f_0}{f_H}\right)$$

$A_f(j\omega)$= closed loop gain (sinusoidal steady state response)
A = open loop gain
A_0 = open loop gain in the passband
A_{0f} = closed loop gain in the passband
β = β-box gain
f = frequency [Hz]
f_0 = frequency of phase reversal [Hz]
f_H = high corner frequency, the frequency at which the gain has dropped 3 dB below the passband gain [Hz]
f_L = low corner frequency [Hz]
n = number of high frequency corners at a single frequency f_0 [Hz]

Transfer function for an A box with 3 high frequency corners occurring at different frequencies:

$$A(j\omega) = \frac{A_0}{\left(1 + j\frac{f}{f_{H1}}\right)\left(1 + j\frac{f}{f_{H2}}\right)\left(1 + j\frac{f}{f_{H3}}\right)}$$

IMPEDANCE

FEEDBACK AND INPUT IMPEDANCE

This applies to the A box - β box voltage amplifier circuit shown previously. Note that the addition of feedback in the circuit results in an increase in input impedance by a factor of $(1+\beta A)$.

$$Z_{in\ f} = \frac{V_{in}}{I_{in}} = Z_{in\ A}(1 + b\,A)$$

$Z_{in\,f}$ = input impedance with feedback [Ω]
$Z_{in\,A}$ = input impedance without feedback [Ω]
A = open loop gain
β = β-box gain

FEEDBACK AND OUTPUT IMPEDANCE

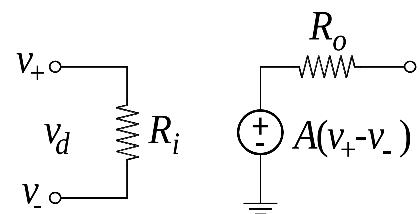
This applies to the A box - β box voltage amplifier circuit shown previously. Note that the addition of feedback in the circuit results in a reduction of output impedance by a factor of $(1+\beta A)$.

$$Z_{out\ f} = \frac{V_{out\ o/c}}{I_{out\ s/c}} = \frac{Z_{out\ A}}{1 + b\,A}$$

$Z_{out\,f}$ = output impedance with feedback [Ω]
$Z_{out\,A}$ = output impedance without feedback [Ω]
$V_{out\,o/c}$ = open circuit output voltage [V]
$I_{out\,s/c}$ = short-circuit output current [A]
A = open loop gain
β = β-box gain

L FINDING LOOP GAIN

1) Model the op amp like this:



2) If the circuit is parallel input (signal enters negative op amp input) convert the input source to a Norton equivalent. If this circuit is series input, use a Thèvenin equivalent source.
3) Redraw the circuit using 1) and 2).
4) Separate the circuit by breaking the feedback loop, usually on the output side of the feedback resistor.
5) Find the Thèvenin equivalent of the output half of the circuit from the perspective of the point at which the circuit was broken in 4). Replace (v_+-v_-) with v_t.
6) Turn off the input source and simplify the input half of the circuit, preserving the nodes v_+ and v_-, corresponding to the op amp inputs, and label the voltage between them v_d.
7) Redraw the circuit using 5) and 6), reconnecting the two halves.
8) Using voltage division, find an equivalent expression for v_d. Solve this expression for v_d/v_t. This is the loop gain L and should be negative.

IMPEDANCE with Z_{ISO}, Z_{IPO}, Z_{OSO}, and Z_{OPO}

Z_{iso} for series input amplifiers (the input signal is going into the **positive** input), the impedance with the input source removed as seen looking into R_{gen}, and takes both R_{gen} and R_o into account.

$$Z_{in} = (1-L)Z_{iso} - R_{gen}$$

Z_{ipo} for parallel input amplifiers (the input signal is going into the **negative** input), the impedance with the sources off and takes both R_{gen} and R_o into account.

$$Z_{in} = \cfrac{1}{\cfrac{1-L}{Z_{ipo}} - \cfrac{1}{R_{gen}}}$$

Z_{oso} for series output amplifiers (amplifier is acting as a **current source**, R_L does not connect to ground), the impedance with sources off as seen looking out of the op amp through R_o, and R_L and also taking R_{gen} into account.

$$Z_{out} = (1-L)Z_{oso} - R_L$$

Z_{opo} for parallel output amplifiers (R_L connects to ground), the impedance with sources off as seen looking through into the output terminals with R_L in place and taking R_o and R_{gen} into account.

$$Z_{out} = \cfrac{1}{\cfrac{1-L}{Z_{opo}} - \cfrac{1}{R_L}}$$

The use of Z_{iso}, Z_{ipo}, Z_{oso}, and Z_{opo} permit impedance calculations for amplifiers whose gain is affected by the input and output loads. Note that the word "sources" used here refers to the input source and to voltage source A inside the op amp. Refer to previous section for finding loop gain L.

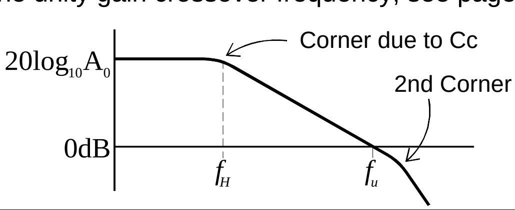
FREQUENCY

OP AMP FREQUENCY RESPONSE

There are no coupling capacitors or bypass capacitors in an op amp, so there are no low frequency corners. That is, the passband gain extends all the way to DC.

There are several high frequency corners, but one of them (due to Cc) is very much lower than the other corners

f_u is the unity gain crossover frequency, see page 9.



FREQUENCY COMPENSATION to achieve AMPLIFIER STABILITY

An amplifier is unstable if 180º phase reversal occurs at a frequency where the gain is 1 V/V or greater. Viewed on a Nyquist plot, this situation occurs when the plot encircles the point (-1, 0). Oscillation will occur. There are several ways to stabilize the amplifier:

1. **Gain reduction** - Reduce the overall gain to obtain a gain margin of 10 dB at the frequency of phase reversal.
2. **Phase Lag compensation** – Keep all the gain magnitude and sacrifice bandwidth. This is done by adding an additional high frequency corner—at a very low frequency. This method is used when none of the existing corners can be lowered, as in an op amp where circuitry is internal.

Original Loop Gain Transfer Function:

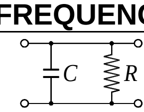
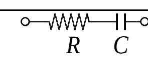
$$-L(j\omega) = \frac{K}{\left(1 + j\frac{f}{10^6}\right)^3}$$

Phase-Lag compensated Loop Gain Transfer Function:

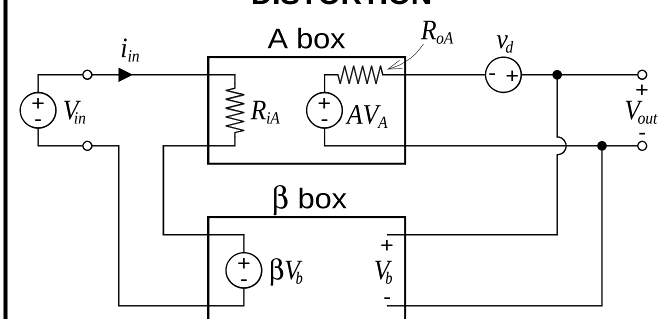
$$-L(j\omega) = \frac{K}{\underbrace{\left(1 + j\frac{f}{10}\right)}_{\text{Added frequency corner}}\left(1 + j\frac{f}{10^6}\right)^3}$$

3. **Lead-lag** method – Reduce the frequency of the lowest frequency corner. This raises the bandwidth by an amount equal to the difference between the two lowest corners (previous to compensation). This can be the most effective method, but is useless if the two corner frequencies are identical.

FREQUENCY CORNER

$f_H = \frac{1}{2\pi RC}$ 	$f_L = \frac{1}{2\pi RC}$ 

DISTORTION



$$V_{out} = \frac{A}{1+\beta A}V_{in} + \frac{1}{1+\beta A}v_d$$

BJTs

h PARAMETERS

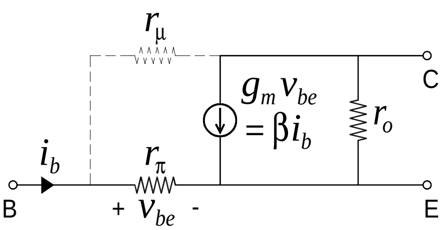
$$h_{fe} = \beta = \frac{I_C}{I_B} = g_m r_\pi = \frac{I_C}{V_T} r_\pi \qquad h_{re} = \frac{r_\pi}{r_\pi + r_\mu}$$

$$h_{ie} = r_\pi = \frac{1}{g_i} = \frac{V_T}{I_B} \qquad \frac{1}{h_{oe}} = r_0 = \frac{V_A}{I_C} = \frac{1}{g}$$

BJT MODELS

HYBRID P

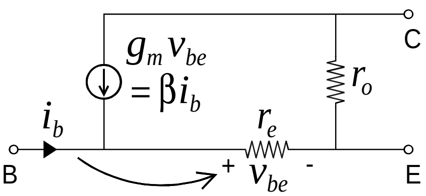
r_m is often taken to be infinite



HYBRID T

r_e is related to r_p by a shift of position in the circuit and

$r_e = r_\pi / (\beta + 1)$



g_f FORWARD TRANSCONDUCTANCE

The forward transconductance varies with the offset voltage and is at a maximum ($g_{f\,max}$) when the offset voltage is zero.

$$g_f \equiv \frac{\partial I_C}{\partial V_{BE}}$$

$$\boxed{g_f = g_m = \frac{I_C}{V_T}}$$

g_f = forward transconductance [A/V]
I_C = collector current [A or mA]
V_i = differential input voltage [V]
V_{BE} = base to emitter voltage [V]
V_T = thermal voltage, typically 26 mV

g_i INPUT TRANSCONDUCTANCE

The conductance looking into the input.

$$g_i \equiv \frac{\partial I_B}{\partial V_{BE}}$$

$$\boxed{g_i = \frac{1}{h_{ie}} = \frac{I_B}{V_T}}$$

g_i = input transconductance [A/V]
h_{ie} = ratio of thermal voltage to base current [Ω]
I_B = base current [A]
V_i = differential input voltage [V]
V_{BE} = base to emitter voltage [V]
V_T = thermal voltage, typically 26 mV

g SOURCE CONDUCTANCE

The conductance looking into the collector.

$$\boxed{g = \frac{I_C}{V_A}}$$

g = source conductance [A/V]
I_C = collector current [A]
V_A = Early voltage [V]

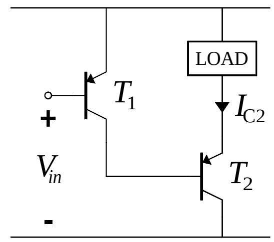
g_o CURRENT SOURCE CONDUCTANCE

The parallel conductance used to model the imperfection of a constant current source.

$g_{f\,darl}$, $g_{i\,darl}$ DARLINGTON CONDUCTANCES

$$g_{f\,darl} \equiv \frac{\partial I_{C2}}{\partial V_{in}} = \frac{I_{C2}}{2V_T}$$

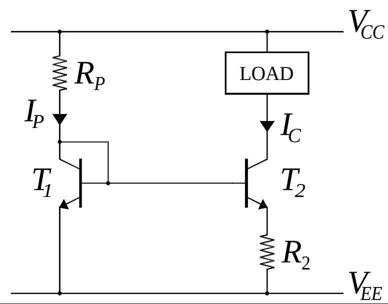
$$g_{i\,darl} \equiv \frac{\partial I_{B1}}{\partial V_{in}} = \frac{I_{B1}}{2V_T}$$



CURRENT MIRRORS

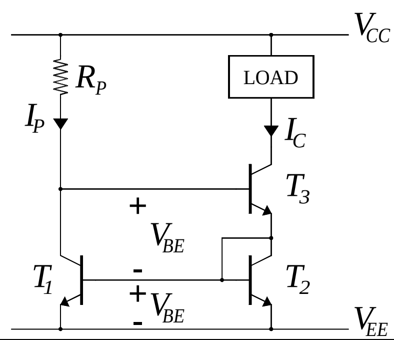
WIDLAR CURRENT SOURCE

The Widlar Current Source is a means of providing a low-level current source without the use of high-value resistors.



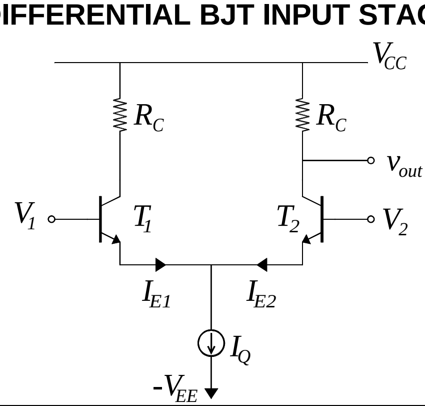
WILSON CURRENT MIRROR

The Wilson Current Mirror substantially improves current regulation and thereby improves the CMRR of the differential amplifier.



BJT INPUT STAGES

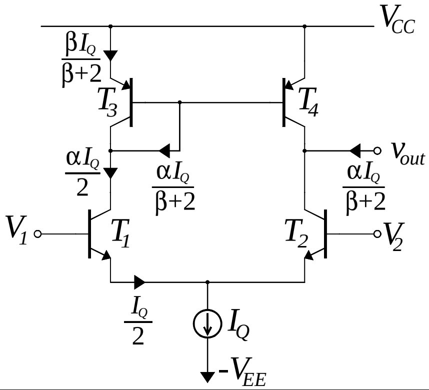
DIFFERENTIAL BJT INPUT STAGE



#1 IMPROVED BJT INPUT STAGE

Collector resistors are replaced with a current mirror in this differential BJT input stage.

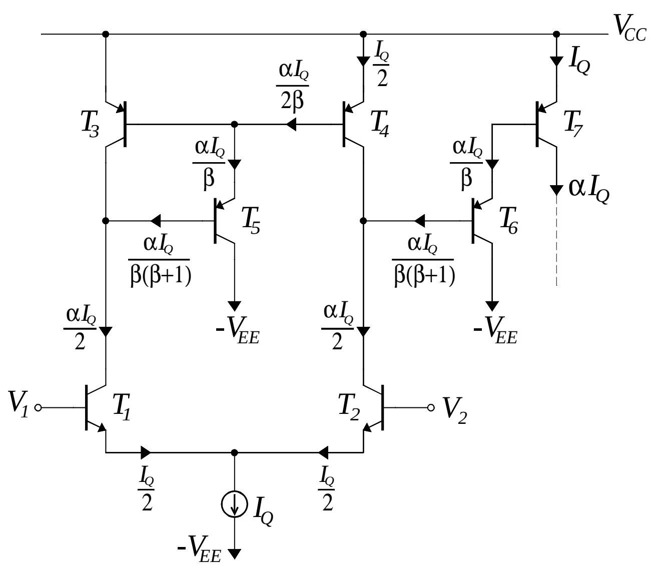
$$A_1 = \frac{2g_{f\,\max}}{g_2 + g_4 + g_{i\,2nd\,stage}} = \frac{2 \times \frac{\alpha I_Q}{4V_T}}{\frac{\alpha I_Q}{2V_A} + \frac{\alpha I_Q}{2V_A} + g_{i\,2nd\,stage}}$$



#2 IMPROVED BJT INPUT STAGE

Differential BJT input stage with **active loads**, shown with darlington second stage. The addition of T_5 in the current mirror reduces the base current to T_6 by approximately a factor of β. DC currents are shown, and are approximate.

$$A_1 = \frac{2g_{f\,\max}}{g_2 + g_4 + g_{i\,darl}} = \frac{2 \times \frac{\alpha I_Q}{4V_T}}{\frac{\alpha I_Q}{2V_A} + \frac{\alpha I_Q}{2V_A} + \frac{\alpha I_Q}{\beta_6(\beta_7+1)2V_T}}$$



DIFFERENTIAL INPUT GAIN

$$A_1 = \frac{2g_{f\,\max}}{g_2 + g_4 + g_{i\,darl}} = \frac{2 \times \frac{I_{C2}}{2V_T}}{\frac{I_{C2}}{V_A} + \frac{I_{C4}}{V_A} + \frac{I_{B\,1st\,darlington}}{2V_T}}$$

$Z_{in\,diff}$ DIFFERENTIAL INPUT IMPEDANCE

$$\boxed{Z_{in\,diff} = 2h_{ie} = \frac{4(\beta+1)V_T}{I_Q}}$$

g_f, $g_{f\,max}$ FORWARD TRANSCONDUCTANCE of a DIFFERENTIAL INPUT AMPLIFIER

The **differential input amplifier** can be thought of as a transconductance amplifier (VCCS).

$$g_f = \left|\frac{\partial I_C}{\partial V_i}\right|$$

$$g_f = \frac{I_{C1} I_{C2}}{\alpha I_Q V_T}$$

$$\boxed{g_{f\,\max} = \frac{\alpha I_Q}{4V_T}}$$

g_f = forward transconductance [A/V or mA/V]
I_C = collector current [A or mA]
V_i = differential input voltage [V]
V_T = thermal voltage, typically 26 mV
α = β/(β+1) ratio of collector current to emitter current.
I_Q = differential current source [A or mA]

g_{cm} COMMON MODE TRANSCONDUCTANCE of a DIFFERENTIAL INPUT AMPLIFIER

The **differential input amplifier** can be thought of as a transconductance amplifier (VCCS).

$$\boxed{g_{cm} = \frac{\Delta I_C}{\Delta V_{CM}} = \frac{\alpha g_o}{2}}$$

g_{cm} = common mode transconductance [A/V]
I_C = collector current [A]
V_{CM} = common mode input voltage [V]
α = β/(β+1) ratio of collector current to emitter current.
g_o = current source conductance [A/V]

CMRR COMMON MODE REJECTION RATIO

The **ratio** of differential gain to common mode gain.

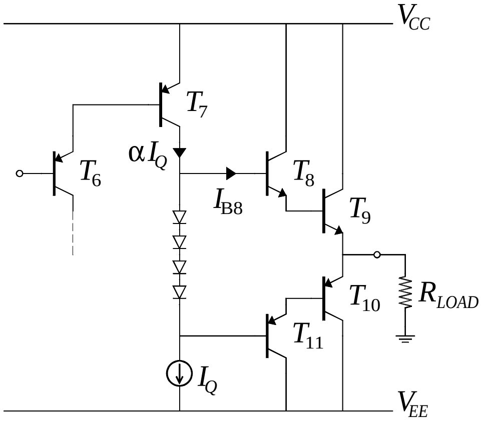
$$\boxed{CMRR = \frac{|A_d|}{|A_{cm}|} = \frac{g_f}{g_{cm}}}$$

in dB: $CMRR = 20\log\frac{|A_d|}{|A_{cm}|}$

A_d = differential gain
A_{cm} = common mode gain
g_f = forward transconductance [A/V]
g_{cm} = common mode trans-conductance [A/V]

BJT 2ND STAGES

2nd STAGE AND OUTPUT STAGE



2nd STAGE GAIN (DARLINGTON PAIR)

Referring to the circuit diagram above, the second stage consists of T_6 and T_7 in a darlington configuration which is associated with the $g_{f\,darl}$ term. The output also uses darlington pairs for the positive- and negative-going signals. This is the reason for squaring the (β+1) term.

$$A_2 = -g_{f\ darl} R_{CE\ load} = -g_{f\ 6,7} \left\{ \left[(\beta+1)^2 R_L \right] \middle\| \frac{1}{g_7} \right\}$$

$$A_2 = -\overbrace{\frac{\alpha I_Q}{2V_T}}^{g_{f\ darl}} \underbrace{\left\{ \left[(\beta+1)^2 R_L \right] \middle\| \overbrace{\frac{V_A}{\alpha I_Q}}^{1/g_7} \right\}}_{\text{Resistive load placed on 2nd stage by output stage.}}$$

see Darlington Conductances on page 7.

2nd STAGE GAIN (SINGLE TRANSISTOR) as in the LM 351 on p 11.

$$A_2 = -g_{f5} R_{CE\ load} = -\frac{I_{C5}}{|V_P|} \left\{ \left[(\beta_7+1) R_L \right] \middle\| \frac{1}{g_5} \right\}$$

$$= -\frac{\beta_5 I_Q}{(\beta_5+2)|V_P|} \left\{ \left[(\beta_7+1) R_L \right] \middle\| \frac{V_{A\ BJT}}{\beta I_Q / (\beta+2)} \right\}$$

C_{mi} MILLER EFFECT CAPACITANCE
f_H DOMINANT FREQUENCY CORNER

The **Miller Effect capacitance** in stage two of the three-stage op amp is responsible for the dominant (lowest) high frequency corner of the op amp. Other corners are present but are too high to be of concern.

$$\boxed{C_{mi} = C_C (1-K)}$$

$$K = A_2$$

$$\boxed{f_H = \frac{1}{2\pi C_{mi} R_{mi}}}$$

$$R_{mi} = \frac{1}{g_2 + g_4 + g_{i\,darl}}$$

C_{mi} = Miller capacitance [F]
C_C = Miller effect capacitance [F]
f_H = the dominant (lowest) high frequency corner [Hz]
A_2 = gain of the second stage
R_{mi} = Miller resistance [Ω]

f_u UNITY GAIN CROSSOVER FREQUENCY or GAIN BANDWIDTH PRODUCT

The **unity gain crossover frequency** is the (high) frequency at which the gain has fallen to one.

$$\boxed{f_u = \frac{g_{f\ \max}}{\pi Cc} = A_0 f_H}$$

for small signals (don't use):

$$f_u = \frac{I_Q}{4\pi V_T Cc} = \frac{SR\alpha}{4\pi V_T}$$

Gain can be expressed as a function of f_u. Yes, it is 90º out of phase due to f_H being at around 5 Hz.

$$\frac{V_{out}}{V_{in}} = j \frac{f_u}{f}$$

$g_{f\,max}$ = maximum forward transconductance [A/V]
C_C = Miller effect capacitance [F]
A_0 = open loop passband gain
f_H = the dominant (lowest) high corner frequency (in this case it is associated with capacitance C_C) [Hz]
V_T = thermal voltage, typically 26 mV
SR = slew rate [V/s]

I_S SCALE CURRENT

The scale current or **saturation current** is proportional to the junction area and affects the value of V_{BE}. Scale current is strongly affected by temperature, as a rule of thumb doubling for every 5°C rise in temperature. **BJT saturation** occurs when the transistor is unable to provide a collector current of βI_B, either because the base current is too high or the voltage supply is too low (my definition). The collector to emitter voltage in saturation is typically about 0.2V.

$$\boxed{I_E \simeq I_S e^{V_{BE}/V_T}}$$

$$I_E = I_S \left(e^{V_{BE}/V_T} - 1 \right)$$

$$\ln \frac{I_E}{I_S} = \frac{V_{BE}}{V_T}$$

I_E = emitter current [A or mA]
I_S = scale current or saturation current [A or mA]
V_{BE} = base to emitter voltage [V]
V_T = thermal voltage, typically 26 mV at room temperature

SR SLEW RATE

The **slew rate** is the **maximum rate of change** of the output voltage, or how fast the output voltage changes in response to a large step at the input.

$$\boxed{SR = \frac{I_Q}{C_C}}$$

SR = output voltage rate of change [V/s]
I_Q = bias current [A]
C_C = Miller effect capacitance [F]

$FPBW$ FULL POWER BANDWIDTH

The **full power bandwidth** is the highest frequency at which a rail to rail output is available without distortion.

$$\boxed{FPBW = \frac{SR}{2pV_{RAIL}}}$$

SR = slew rate; output voltage rate of change [V/s]
V_{RAIL} = the maximum voltage to which the output may be driven, usually about 2 volts less than the supply voltage [V]

f_{max} MAXIMUM FREQUENCY

The **maximum frequency** without **slew rate distortion** for a sinewave output signal of V_p volts. Slew rate distortion occurs when the rate of change of the output voltage attempts to exceed the slew rate (the maximum rate of the change of the output voltage). The maximum rate of change of a sine wave occurs when the voltage crosses zero. So for a sine wave of frequency f and peak amplitude V_p, $\left(V_p \sin 2\pi ft\right)$, the rate of change at any time in the cycle is given by $\frac{dV_0}{dt} = 2\pi f V_p \cos 2\pi ft$. The slope of this signal will have its maximum amplitude when the cosine term becomes ±1.

$$\boxed{f_{\max} = \frac{SR}{2\pi V_p}}$$

f_{max} = maximum frequency without slew rate distortion [Hz]
SR = output voltage rate of change [V/s]
V_p = peak output voltage [V]

f_{Hf} SMALL SIGNAL BANDWIDTH

Since the **gain bandwidth product** remains constant, the application of feedback reduces the gain and increases the bandwidth by the same factor of $(1+\beta A_0)$.

$$\boxed{f_{Hf} = \left(1+\beta A_0\right) f_H}$$

where $\beta = \frac{R_1}{R_1 + R_f}$

(Add R_g to R_1 if present.)

f_{Hf} = small signal bandwidth, or high frequency corner with feedback [Hz]
β = b box gain
A_0 = open loop gain in the passband
$f_H = f_u/A_0$ high freq. corner [Hz]

V_{iN} NORMALIZED INPUT VOLTAGE

The input voltage is normalized to unity to use in plotting normalized emitter/drain currents versus normalized input voltages in a **differential amplifier**.

$$\boxed{V_{iN} = \frac{V_i}{V_P}\sqrt{\frac{I_{DSS}}{I_Q}}}$$

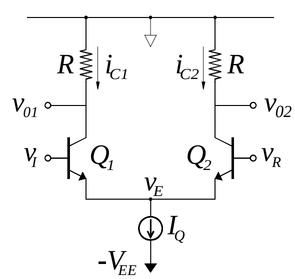
V_i = differential input voltage [V]
V_P = peak output voltage [V]
I_{DSS} = drain to source scale current or saturation current? [A]
I_Q = bias current [A]

EMITTER COUPLED LOGIC

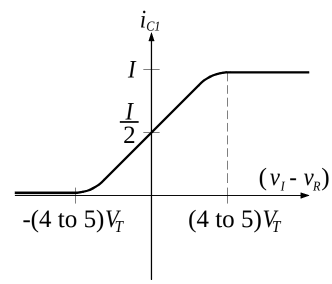
With v_R taken to be a reference, the circuit below functions as an inverter with input v_I and output v_{01}. The advantage to this circuit is that the collector currents (one or the other) become saturated without much charge on the base, permitting fast operation

$\boxed{i_{C1} = I_S e^{(v_I - v_E)/V_T}}$ $\boxed{i_{C2} = I_S e^{(v_R - v_E)/V_T}}$ where $V_T = \frac{kT}{q}$

I_S = scale current [A]
I_Q = bias current [A]



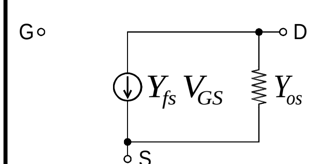
Transfer Characteristic



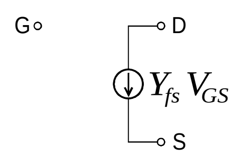
JFETs

CIRCUIT MODEL

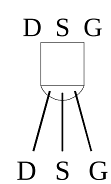
MODEL



SIMPLE MODEL



D drain, S source, G gate
Y_{fs} = forward transconductance [Ω^{-1}]
Y_{os} = slope of the output characteristic [Ω^{-1}]
I_{DSS} = scale current or saturation current? [A]
V_{GS} = gate-to-source voltage [V]
V_P = pinchoff voltage, the highest voltage at which there is still no drain current [V]



Y_{fs} FORWARD TRANSCONDUCTANCE

$$Y_{fs} \equiv \frac{\partial I_D}{\partial V_{GS}} \qquad \boxed{Y_{fsQ} = \left|\frac{2I_{DSS}}{V_P}\right|\left[1-\frac{V_{GS}}{V_p}\right]}$$

Y_{fs} = slope of the FET transfer characteristic [A]
I_{DSS} = scale current or saturation current? [A]
V_{GS} = gate-to-source voltage [V]
V_P = pinchoff voltage, the highest voltage at which there is still no drain current [V]

I_D DRAIN CURRENT

$$\boxed{I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_p}\right]^2}$$

I_{DSS} = scale current or saturation current? [A]
V_{GS} = gate-to-source voltage [V]
V_P = pinchoff voltage, the highest voltage at which there is still no drain current [V]

$g_{f\,max}$ JFET MAXIMUM FORWARD TRANSCONDUCTANCE

$$\boxed{g_{f\,\max} = \frac{\sqrt{I_{DSS} I_Q / 2}}{|V_P|}}$$

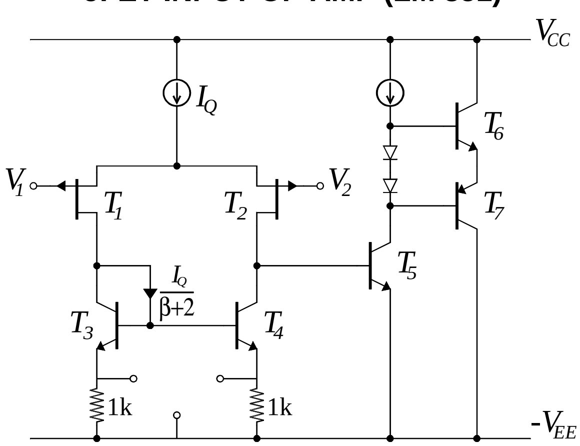
I_{DSS} = drain to source scale current or saturation current? [A]
I_Q = differential amplifier supply current [A]
V_P = pinchoff voltage [V]

Y_{os} JFET OUTPUT ADMITTANCE

$$Y_{os} \equiv \frac{\partial I_D}{\partial V_{DS}} \qquad Y_{os} = \frac{1}{r_o} = \frac{I_D}{V_A}$$

Y_{os} = slope of the output characteristic [Ω^{-1}]
I_D = drain current [A]
V_{DS} = drain to source voltage [V]
V_A = Early voltage, typically 100V [V]

JFET INPUT OP AMP (LM 351)

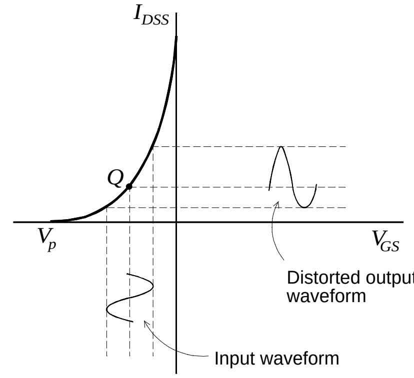


DIFFERENTIAL INPUT GAIN (with FETs)

$$A_d = \frac{2g_{f\,\max}}{g_2+g_4} = \frac{\dfrac{2\sqrt{I_{DSS}I_Q/2}}{|V_P|}}{4V_T} \div \left(\frac{I_Q/2}{V_{A\,JFET}}+0\right)$$

HARMONIC DISTORTION

Harmonic distortion is caused by the non-linearity of the **transfer characterictic**.



V_{out} has the form

$$V_{out} = A_0 + A_1\sin(\omega t+\phi_1) + A_2\sin(2\omega t+\phi_2)+\cdots$$

The percent second harmonic distortion would be

$$\boxed{D_{2H} = \frac{A_2}{A_1}\times 100}$$

For the JFET, since the drain current is proportional to the output voltage, substitute

$$V_{GS} = V_{GSQ} + V_{in}\sin\omega t \quad \text{into} \quad I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_p}\right]^2$$

We are only interested in the terms formed by the values within the parenthesis. Use the trig identity

$$\sin^2\omega t = \frac{1}{2}-\frac{1}{2}\cos 2\omega$$

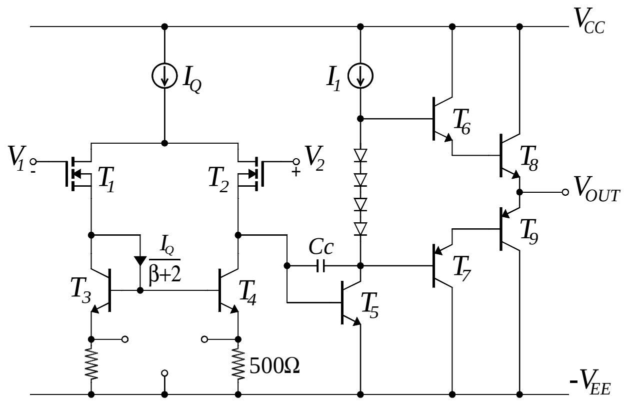
(It doesn't matter, for distortion purposes, whether it's sine or cosine.)

MOSFETs

MOSFET INPUT STAGE CHARACTERISTICS

- very low input current (a few pA)
- very high Z_{in} (up to $10^{15}\Omega$)
- reasonable f_u and slew rate
- high offset voltages (tens of mV)
- high noise
- vulnerable to static electricity

MOSFET INPUT OP AMP



i_D MOSFET DRAIN CURRENT

NMOS triode region $\quad i_{Dn}=\frac{1}{2}k_n'\left(\frac{W}{L}\right)_n\left[2\left(v_{GS}-V_{tn}\right)-v_{DS}\right]V_{DS}$

NMOS saturation $\quad i_{Dn}=\frac{1}{2}k_n'\left(\frac{W}{L}\right)_n\left(v_{GS}-V_{tn}\right)^2$

PMOS triode region $\quad i_{Dp}=\frac{1}{2}k_p'\left(\frac{W}{L}\right)_p\left[2\left(v_{SG}-\left|V_{tp}\right|\right)-v_{SD}\right]V_{SD}$

PMOS saturation $\quad i_{Dp}=\frac{1}{2}k_p'\left(\frac{W}{L}\right)_p\left(v_{SG}-\left|V_{tp}\right|\right)^2$

k' = process transconductance parameter [mA/V^2]
W/L = channel width to length ratio
v_{GS} = gate-to-source voltage [V]
V_{tn}, V_{tp} = threshhold voltage [V]
v_{DS} = drain-to-source voltage [V]
v_{SD} = source-to-drain voltage [V]

Point of Confusion: An NMOS transistor leaves the **saturation region** and enters the **triode region** when the gate voltage has reached a level such that further increases do not produce additional drain current. This is essentially the opposite of the definition for saturation current in a BJT. For the NMOS transistor we have:

triode region	**saturation region**
$v_{GS}>v_{DS}+V_t$	$v_{GS}\le v_{DS}+V_t$

MOSFET SATURATION

This is much different from BJT saturation as it occurs when the gate voltage is low. The MOSFET is in saturation when the gate voltage is less than the sum of the drain-to-source voltage and the threshold voltage.

Saturation:	**Triode region:**
$\boxed{v_{GS}<v_{DS}+V_t}$	$\boxed{v_{GS}\ge v_{DS}+V_t}$

$g_{f\,max}$ MOSFET MAXIMUM FORWARD TRANSCONDUCTANCE

$$\boxed{g_{f\max}=\sqrt{\frac{KI_Q}{2}}}$$

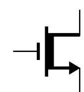
K = process transconductance parameter [mA/V^2]
I_Q = differential amplifier supply current [A]

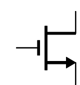
A_1 MOSFET INPUT STAGE GAIN

$$A_1=\frac{2g_{f\max}}{g_{total}}=\frac{2g_{f\max}}{g_2+g_5}=2\sqrt{\frac{KI_Q}{2}}\div\left(\frac{I_Q}{2V_{A\,mosfet}}+\frac{I_{B5}}{V_T}\right)$$

DEPLETION-TYPE MOSFET

An n-channel (NMOS) depletion-type MOSFET already has a channel formed with no gate voltage applied. To turn off the transistor, a negative gate voltage is applied. So the threshold voltage is negative. The enhancement-type NMOS transistor requires a positive gate voltage for the device to conduct.

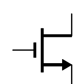
NMOS depletion-type: 

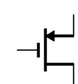
NMOS enhancement-type: 

CMOS

CMOS – Complementary Metal Oxide Silicon

CMOS technology employs the use of both NMOS and PMOS transistor types for greater design flexibility. The disadvantage to CMOS is its low current-handling ability. This problem is overcome by the use of **BiCMOS** technology—the combination of CMOS and BJT devices.

NMOS: 

PMOS: 

NOISE

NOISE – Any unwanted signal

Electronic noise is the type of noise we will study. It can be minimized but not eliminated.

Noise referral is the practice of quantifying by determining the level of noise at the input that would produce the amount of noise in question. (*refer to document* **NoiseReferral.pdf**)

Shot noise (Schottky noise) is due to a random number of carriers participating in current flow across a p-n junction. This is a **white noise**, meaning it has a uniform power spectral density (noise power per hertz). Base current has a shot noise component.

Thermal noise or **Johnson noise** occurs in resistors and is due to the thermal aggitation of free electrons in the resistor material. Net movement is zero but at times electrons are moving one way or the other. Thermal noise is also white noise.

Excess noise or **flicker noise** occurs in resistive material when a DC current flows through it. It is in excess of thermal noise.

i_n NOISE COMPONENT and BANDWIDTH

The noise component of an average current I_Q is given by

$$\boxed{i_n = \sqrt{2qI_Q B}}$$

$$\boxed{B = \frac{\pi}{2} f_H}$$

i_n = noise [$\mathbf{A}/\sqrt{\mathbf{Hz}}$]
q = electron charge 1.602×10^{-19} C
I_Q = differential amplifier supply current [A]
B = the subsequent **noise bandwidth** which follows in the amplifier [Hz]

V_n THERMAL NOISE

Occurs in resistors due to the thermal agitation of free electrons

$$\boxed{V_n = \sqrt{4kTRB}}$$

V_n = thermal noise [V_{rms}]
k = Boltzman's constant 1.38×10^{-23} J/K
T = temperature [K]
R = resistance [Ω]
B = the subsequent **noise bandwidth** which follows in the amplifier [Hz]

V_{ni} TOTAL BJT NOISE IN A DIFFERENTIAL PAIR

Occurs in BJT transistors due to thermal noise in the base spreading resistance and shot noise in the collector current (referred to the input).

$$\boxed{V_{ni} = \sqrt{\underbrace{8kTr_{bb'}}_{\text{base spreading}} + \underbrace{16V_T^{\,2}\left(q/\alpha I_Q\right)}_{\text{shot noise referred to input}}}}$$

V_{ni} = (BJT) differential input noise [$\mathbf{V}/\sqrt{\mathbf{Hz}}$]
$r_{bb'} = r_x$ base spreading resistance [Ω]

V_{ni} FET INPUT NOISE

Occurs in FET transistors due thermal noise in the channel

$$\boxed{V_{ni} = \sqrt{4kT\left(\frac{2}{3Y_{fs}}\right)}}$$

V_{ni} = (FET) input noise [$\mathbf{V}/\sqrt{\mathbf{Hz}}$]
Y_{fs} = maximum forward transconductance [A/V]

i_{ex} EXCESS NOISE

Excess noise or **flicker noise** occurs in resistive material when a DC current flows through it. It is in excess of thermal noise. It is dependent on the type of resistive material and varies with frequency. It is normally measured (not calculated).

$$i_{ex} = \sqrt{\frac{KI_{DC}B}{f}}$$

K = a constant, dependent on material
I_{DC} = current in the resistor [A]
B = the subsequent noise bandwidth (which follows in the amplifier [Hz]

NF NOISE FIGURE

The ratio of total noise (referred to the input) to the noise due to the impedance of the input device (R_g).

$$\boxed{NF = 10\log_{10}\frac{V_a^{\,2}}{4kTR_g}}$$

NF = noise figure [dB]
$V_a^{\,2}$ = equivalent input noise squared [V^2/Hz]
k = Boltzman's constant 1.38×10^{-23} J/K
T = temperature [K]
R_g = source impedance [Ω]

V_{no} NOISE VOLTAGE AT THE OUTPUT

The noise level at the output, assuming uniform spectral noise density and given the noise bandwidth.

$$\boxed{V_{no} = V_a\sqrt{B}}$$

V_{no} = noise voltage at the output [V]
V_a = equivalent input noise squared [$\mathbf{V}/\sqrt{\mathbf{Hz}}$]
B = **noise bandwidth** [Hz]

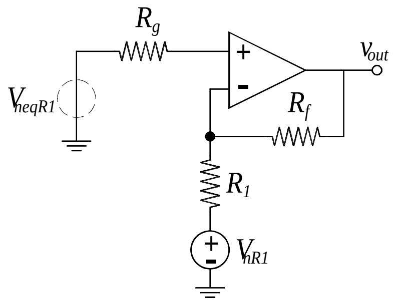
SNR SIGNAL TO NOISE RATIO

$$SNR = 20\log_{10}\frac{V_S}{V_N} \qquad NF = SNR_i - SNR_o$$

NOISE REFERRAL

All noise in the amplifier system is converted to an **equivalent input noise**, i.e. the level of noise at the input which would result in the level of noise under study. The example below shows how to refer the noise in resistor R_1 to an equivalent input noise.

V_{neqR1} is multiplied by the gain of the amp to give the noise at the output. Likewise, V_{nR1} (the noise in R_1) sets up a current through R_1 and goes to ground at the op amp input (asymetric conditions). Since this current cannot flow into the op amp, it flows through R_f, developing a voltage at the output. Although this voltage will be negative, it may be considered positive since it will be squared later. Refer to Thermal Noise to calculate V_{nR1}.

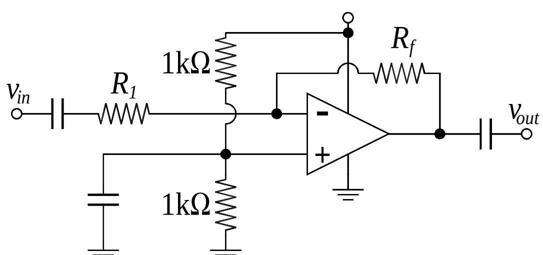


$$V_{neqR1}\frac{R_1+R_f}{R_1} = V_{out} = -\frac{R_f}{R_1}V_{nR1}$$

SINGLE-SUPPLY AMPLIFIERS

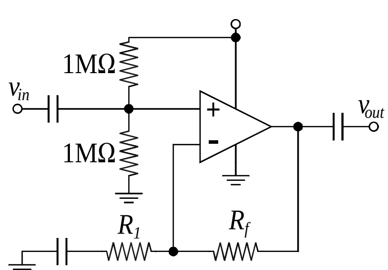
INVERTING

The inverting amplifier has less noise than the non-inverting amplifier due to the lower value (1k) of resistors that bring the DC input level to mid-supply, and the fact that the capacitor connected to their midpoint shunts noise to ground. The main consideration in sizing these would be current drain.



NON-INVERTING

This amplifier is very noisy due to the two 1MΩ resistors that are used to bring the DC input level to mid-supply. Reducing the value of these resistors would lower the input impedance.



VOLTAGE OFFSET

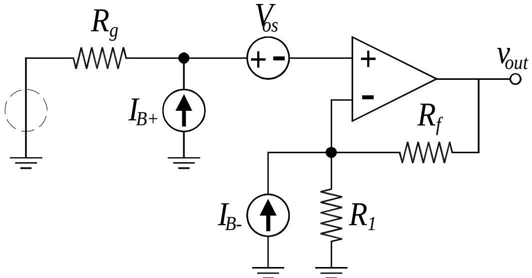
FINDING THE VOLTAGE OFFSET

It is desired that the output voltage be zero in the absence of an input signal. Factors conspiring against this are rated in terms of

- V_{os} - input offset voltage,
- I_B - input bias current $(I_{B-} + I_{B+})/2$
- I_O - input offset current $|I_{B-} - I_{B+}|$

To find the resulting output voltage offset, a model is created and the effect of the three inputs, V_{os+}, I_{B+}, & I_{B-}, on the output is calculated. To find the **worst case**, the offset voltage source and the larger of the two current sources are applied to the input where they will do the most harm. For both the inverting and non-inverting amplifiers, this seems to be the **positive input**, provided that it is not tied to ground.

NON-INVERTING OFFSET MODEL

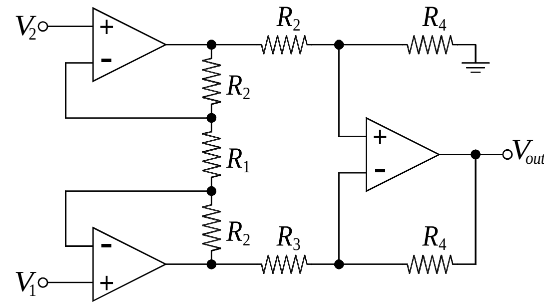


The offset voltage is equal to the voltage at the positive input multiplied by the gain, added to the voltage at the output resulting from current I_{B-}. For the **worst case offset** for this amplifier, let $I_{B+} = I_{B-} + I_O$.

$$V_{out\ offset} = \frac{R_f + R_1}{R_1}\left(V_{ox} + I_{B+}R_g\right) - I_{B-}R_f$$

INSTRUMENTATION AMPLIFIER

This type of amplifier has high gain (10^5 or so) and high common mode rejection ratio (> 100 dB) for the amplification of very weak signals. Gain can be controlled by the value of R_1.

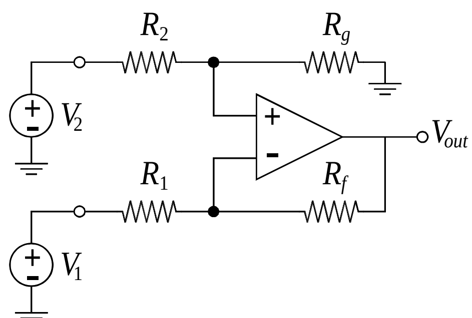


$$A_{diff} = \frac{R_4}{R_3}\left(1 + 2\frac{R_2}{R_1}\right)$$

DIFFERENTIAL OP-AMP AMPLIFIERS

SINGLE OP-AMP DIFFERENTIAL AMPLIFIER

This is not a true **differential amplifier** since the output is a weighted difference, unless we set $R_f / R_1 = R_g / R_2$. When calculating differential gain, $V_1 = V_{in}/2$ and $V_2 = -V_{in}/2$.



By superposition, the output is $V_{\text{out V1}} + V_{\text{out V2}}$.

$$V_{out\,V1} = -\frac{R_f}{R_1}v_1 \qquad V_{out\,V2} = \underbrace{\frac{R_1 + R_f}{R_1}}_{\text{gain}} \times \underbrace{\frac{R_g}{R_2 + R_g}}_{\text{by voltage division}} V_2$$

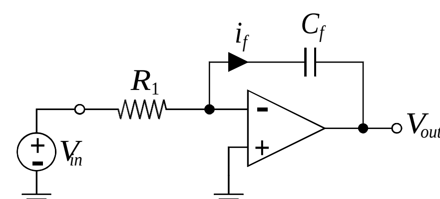
Differential gain: $A_{diff} = \dfrac{V_{out\,V2} - V_{out\,V1}}{V_2 - V_1} = \dfrac{A_2 - A_1}{2}$

For **common mode gain**, $V_1 = V_2 = V_{\text{cm}}$ and

$$A_{cm} = \frac{V_{1\,out\,cm} + V_{2\,out\,cm}}{V_{cm}} = A_1 + A_2$$

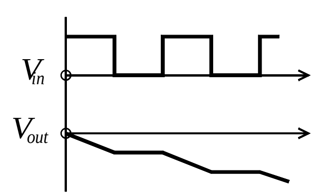
FILTERS

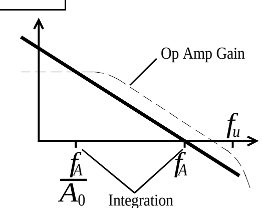
INTEGRATOR



$$V_{out} = -\frac{1}{C_f}\int_0^t i_f\ dt = -\frac{1}{C_f}\int_0^t \frac{V_{in}}{R_1}\ dt = -\frac{1}{C_f R_1}\int_0^t V_{in}\ dt$$

$$\boxed{V_{out} = -\frac{1}{C_f R_1}\int_0^t V_{in}\ dt + \underbrace{V_{out}(0)}_{\text{initial capacitor charge}}} \qquad f_A = \frac{1}{2\pi C R_1}$$



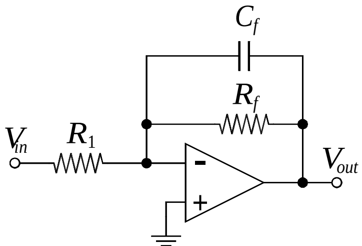


Gain: $\dfrac{V_{out}}{V_{in}}(j\omega) = -\dfrac{Z_C}{R_1} = \dfrac{-1/\,j\omega C}{R_1} = j\dfrac{1}{2\pi f C R_1}$

LEAKY INTEGRATOR

The leaky integrator is a 1st **order low-pass filter**. The order of a filter refers to the order of the polynomial in the denominator of the transfer function and usually corresponds to the number of frequency elements, in this case, one capacitor.

At low frequencies, feedback passes (leaks) through R_f and at high frequencies feedback passes through C_f.

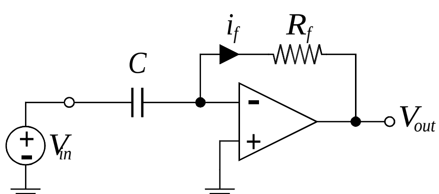


$$\frac{V_{out}}{V_{in}}(j\omega) = -\frac{Z_f}{Z_1} = -\frac{\frac{1}{j\omega C_f}\Big\|R_f}{R_1} = \frac{-\frac{R_f}{R_1}}{1+j\omega C_f R_f}$$

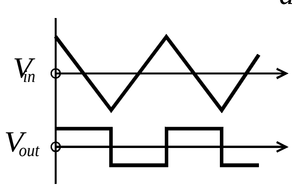
$$\frac{V_{out}}{V_{in}}(j\omega) = \frac{-\frac{R_f}{R_1}}{1+j\frac{f}{f_H}} \qquad \boxed{f_H = \frac{1}{2\pi C_f R_f}}$$

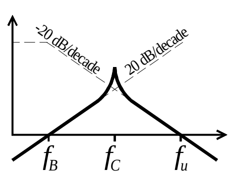
DIFFERENTIATOR

There is lagging phase shift in addition to the op amp's phase shift, so phase reversal can occur when loop gain is less than 1.



$$V_{out} = -i_f R_f = -R_f C\frac{dv_{in}}{dt} \qquad f_C = \sqrt{f_B f_u}$$





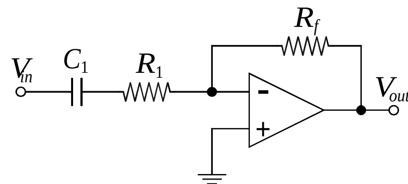
Gain: $\frac{V_{out}}{V_{in}}(j\omega) = -\frac{Z_f}{Z_1} = -\frac{R_f}{\frac{1}{j\omega C}} = -j2\pi f C R_f$

Let $f_B = \frac{1}{2\pi C R_f}$ $\qquad \frac{V_{out}}{V_{in}}(j\omega) = -j\frac{f}{f_B}$

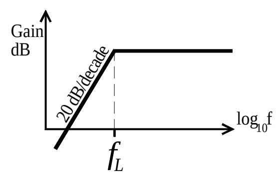
$$\text{gain }(dB) = 20\log_{10} f - 20\log_{10} f_B$$

FIRST ORDER HIGH PASS FILTER

There is lagging phase shift in addition to the op amp's phase shift, so phase reversal can occur when loop gain is less than 1.

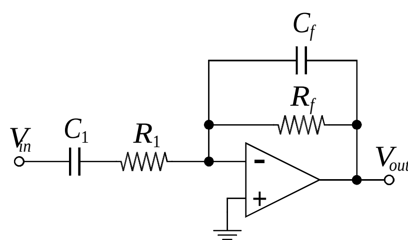


$$\frac{V_{out}}{V_{in}}(j\omega) = -\frac{Z_f}{Z_1} = \frac{-R_f}{R_1+\frac{1}{j\omega C_1}} = \frac{-\frac{R_f}{R_1}}{1-j\frac{1}{\omega C_1 R_1}} = \frac{-\frac{R_f}{R_1}}{1-j\frac{f_L}{f}}$$



$$\boxed{f_L = \frac{1}{2\pi C_1 R_1}}$$

FIRST ORDER BAND PASS FILTER

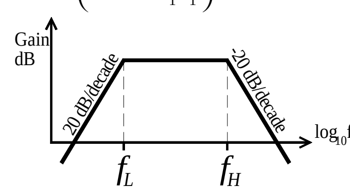


$$\boxed{f_L = \frac{1}{2\pi C_1 R_1}}$$

$$\boxed{f_H = \frac{1}{2\pi C_f R_f}}$$

$$\frac{V_{out}}{V_{in}}(j\omega) = -\frac{Z_f}{Z_1} = -\frac{\frac{1}{j\omega C_f}\Big\|R_f}{R_1+\frac{1}{j\omega C_1}} = \frac{-\frac{R_f}{R_1}}{\left(1-j\frac{1}{\omega C_1 R_1}\right)\left(1+j\omega C_f R_f\right)}$$

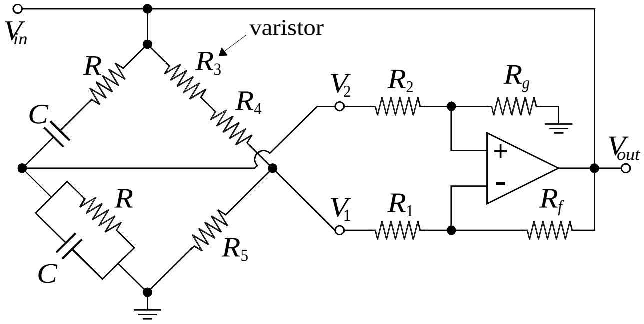
$$= \frac{-\frac{R_f}{R_1}}{\left(1-j\frac{f_L}{f}\right)\left(1+j\frac{f}{f_H}\right)}$$



OSCILLATORS

WEIN BRIDGE OSCILLATOR

This oscillator is capable of very **low frequencies**.



Find V_1 and V_2: $V_1 = V_{in}\dfrac{R_5}{R_3+R_4+R_5}$

$$V_2 = V_{in}\frac{\dfrac{R\times\frac{1}{j\omega C}}{R+\frac{1}{j\omega C}}}{R+\dfrac{1}{j\omega C}+\dfrac{R\times\frac{1}{j\omega C}}{R+\frac{1}{j\omega C}}} = V_{in}\frac{R}{3R+j\left(\omega CR^2-\dfrac{1}{\omega C}\right)}$$

V_2 (and V_{out}) will be in phase with V_{in} when $\omega CR^2 = 1/(\omega C)$ so

$$\omega_0^{\ 2} = \frac{1}{R^2C^2}\,,\quad \omega_0 = \frac{1}{RC}\quad \text{and}\quad f_0 = \frac{1}{2\pi RC}$$

At ω_0, $V_1 = V_{in}\dfrac{R_5}{R_3+R_4+R_5}$ and $V_2 = \dfrac{1}{3}V_{in}$

The loop gain is the 1st *stage* gain × 2nd stage gain:

$$\frac{V_2-V_1}{V_{in}}\times\frac{V_{out}}{V_2-V_1} = \left(\frac{1}{3}-\frac{R_5}{R_3+R_4+R_5}\right)\frac{R_f}{R_1}$$

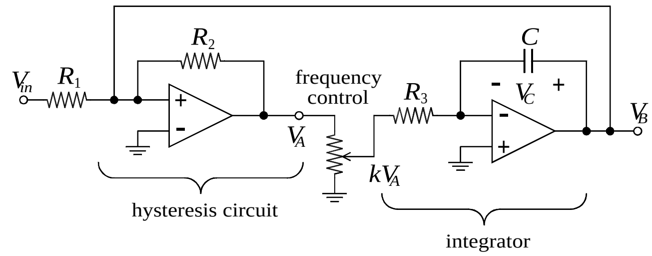
To just sustain oscillations, the loop gain must be 1:

$$\frac{R_1}{R_f} = \frac{1}{3}-\frac{R_5}{R_3+R_4+R_5}$$

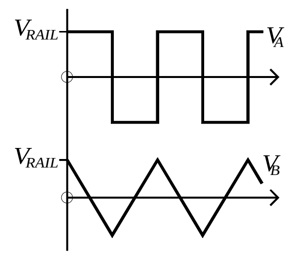
R_3 is a varistor which serves to limit the gain.

FUNCTION GENERATOR

This function generator produces a square wave at V_A, and a triangle wave at V_B. Due to the positive feedback in the 1st IC, V_A will go to one of the rails. If V_A is positive, then to get it to go negative, V_{in+} needs to be slightly negative.



$$V_B = -\frac{kV_{RAIL}}{R_3C}t$$



Frequency of oscillation:

$$\boxed{f_0 = \frac{kR_2}{4R_1R_3C}}$$

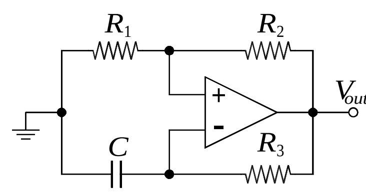
Square wave time to rise:

$$t_R = 0.8\frac{2V_{RAIL}}{SR}$$

ASTABLE MULTIVIBRATOR

$$k = \frac{R_1}{R_1+R_2}$$

$$\tau = R_3C$$



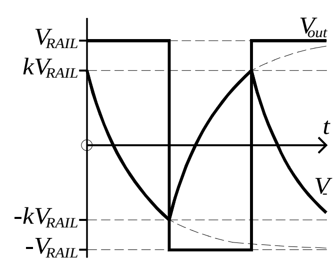
Frequency of oscillation:

$$\boxed{f_0 = \frac{1}{2R_3C\ln\left(\dfrac{1+k}{1-k}\right)}}$$

Rise time is the time it takes to get from 10% to 90% of asymptote and is dependent on the slew rate *SR*.

$$\text{rise time} = \frac{2V_{RAIL}}{SR}\times 0.8$$

V_{out} and V_- Waveforms



CHARACTERISTICS OF THE IDEAL OP AMP

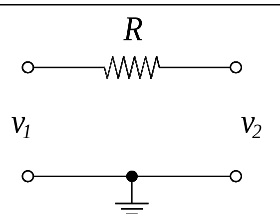
- The difference between the voltages at the inputs (v_2 - v_1) multiplied by the open-loop gain A yields the op amp output $A(v_2 - v_1)$.
- The input impedance is infinite.
- The input current is zero.
- The output impedance is zero.
- The output current is whatever is required to maintain the output voltage.
- The output is in phase with the signal at the positive input.
- Infinite **common-mode rejection**, the rejection of identical signals at the + and - inputs.
- The open-loop gain A is equal for all frequencies.
- The open-loop gain A is infinite.

GRAPHING TERMINOLOGY

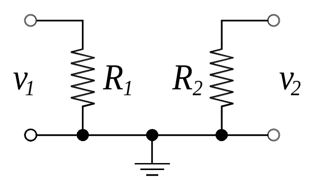
With x being the horizontal axis and y the vertical, we have a graph of ***y* versus *x*** or ***y* as a function of *x***. The x-axis represents the **independent variable** and the y-axis represents the **dependent variable**, so that when a graph is used to illustrate data, the data of regular interval (often this is time) is plotted on the x-axis and the corresponding data is dependent on those values and is plotted on the y-axis.

MILLER THEOREM

The circuit at left may be replaced by the circuit at right. (One of the resistances in the circuit at right will actually be negative).

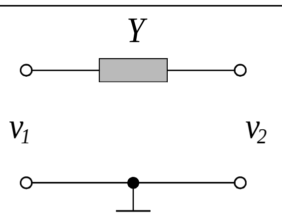


$$K = \frac{v_2}{v_1}$$

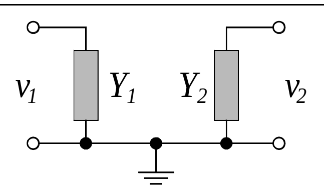


$$R_1 = \frac{R}{1-K}$$
$$R_2 = R - R_1$$

For an admittance Y we have:



$$K = \frac{v_2}{v_1}$$



$$Y_1 = Y(1-K)$$
$$Y_2 = Y(1-1/K)$$

DECIBEL CONVERSION

$$G_{dB} = 20\log_{10} G_{V/V}$$
$$G_{V/V} = 10^{(G_{dB}/20)}$$

G_{dB} = Gain in decibels
$G_{V/V}$ = Gain in volts per volt

DETERMINING IMPEDANCE

TO FIND Z_{in}:

1) Remove the input source.
2) Leave the load connected.
3) Short other independent voltage sources; open other independent current sources.
4) If there are no dependent sources, the input impedance is determined by inspection, otherwise continue to step 5.
5) Keep in mind that current could flow in the circuit. Either a) manipulate the circuit using resistance reflection rule to ground out the independent sources, b) apply a test source to the input, or c) use other Tricks (p.2) to redraw the circuit.

TO FIND Z_{out}:

1) Remove the load .
2) Turn off the input source, but leave the source (resistance) connected.
3) Short other independent voltage sources; open other independent current sources.
4) If there are no dependent sources, the output impedance is determined by inspection, otherwise continue to step 5.
5) Keep in mind that current could flow in the circuit. Either a) manipulate the circuit using resistance reflection rule to ground out the independent sources, b) apply a test source to the output, or c) use other Tricks (p. 2) to redraw the circuit.

MISC.

Voltage across an inductor: $v_L(t) = L\frac{di}{dt}$

Current in an inductor: $i_L(t) = \frac{1}{L}\int_0^t v\, d\tau + i(0)$

Voltage across a capacitor: $v_C(t) = \frac{1}{C}\int_0^t i\, d\tau + v(0)$

Current in a capacitor: $i_C(t) = C\frac{dv}{dt}$

EQUATIONS COMMON TO INDUCTOR & CAPACITOR CIRCUITS

Current: $i(t) = I_f + (I_o - I_f)e^{-t/\tau}$

Voltage: $v(t) = V_f + (V_o - V_f)e^{-t/\tau}$

Power: $p = I_o^{\ 2} R e^{-2t/\tau}$

where
I_0 is initial current [A]
I_f is final current [A]
t is time [s]
τ is the time constant; τ = RC for capacitive circuits, τ = R/L for inductive circuits [s]
V_0 is initial voltage [V]
V_f is final voltage [V]
p is power [W]
R is resistance [Ω]