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Perry Victor Lea

2017 -	**Director of Technology** – Cradlepoint - Office of the CTO • Strategist and evangelist for Cradlepoint IoT, fog compute, SDN networking solutions and advances. • Technical council to C-Level staff. • Senior technical staff to a multi-regional team of 200 engineers. Accountable for strategic development, pathfinding, partnerships and research in advances for IoT & edge compute systems. • Fortune 50 customer facing technologist. Liaison to DoD, NSF and DARPA. Ownership of academic and university relationships in areas of adaptive network security and fog compute. Invited conference speaker and panelist. • Director of intellectual property process, council, and protect growth for IPO candidacy. • Investigator and advisor for mergers and acquisitions. • Chartered with the driving to a 100%+ increase in TAM and SAM through IoT segment advances.
2015-2017	**Director of Strategy and Architecture** – Micron Technology - Advanced Computing Group **Distinguished Member of Technical Staff** • Senior technical council for Micron executive staff and technical lead for staff of 40 (DRAM designers, computer architects, computational mathematicians, logic designers, system architects, and software engineers). • Chartered with team construction and composition. Participated in the merger/acquisition/integration of Convey Computers into group. • Worldwide technical evangelist, business developer and strategist for processing in memory solutions. • Architect of Micron's processing in memory solution. • Managed broad and complex technical partnerships across academia, software providers, silicon partners, and government agencies. • Responsible for pathfinding, roadmaps, architectural definition, business development, design, and delivery of a game changing computing systems directly attacking Moore's Law and Dennard Scaling through processing in memory (PIM) technology within a DRAM process. • Development of new technologies, intellectual property, defensive publications, and creation of new markets for emerging computational memory. • Principle investigator for National Geospatial Intelligence Agency, Microsoft Research, Allen Institute, etc.
2010-2015	**Distinguished Technologist** – Hewlett Packard Co. **Chief Architect of Embedded Systems** • Technical council for executive staff and division vice president/general manager. • Accountable for over 40 cradle to grave product launches. • Strategist and lead for multi-discipline R&D lab comprising 500+ engineers and scientists for HP brand. • Advanced HP's strategic interests through architecting memory technologies, SOC architecture, forming silicon alliances, establishing security systems, advancing memristor storage, ownership of firmware stacks, publications, and building a strong patentable IP portfolio. • Developed and fostered strategic partnerships with: ARM, Vivante, Microsoft, Intel, Marvell, & PMC-Sierra. • Developed and drove innovation from research phase to products in ASICs, imaging, security, and power with Purdue, Rochester Institute of Technology, Boise State University and Columbia University. • Research, design, prototyping, and evangelizing novel imaging, security, multi-touch and display technologies, and embedded technologies pervasive to HP. • Proven ability to cross multiple domains of imaging, electrical engineering, computer science, operations, procurement, marketing, and various business units. • Responsible for the successful delivery 30 million shipping products ranging from consumer to enterprise imaging systems over a 4 year period. • Managed a senior team of 10 master architects involved in hardware, software and firmware design.

2004-2010	**Master Architect of Technical Staff** - Hewlett Packard Co. - Embedded System Laboratory • Principal hardware/firmware architect for Embedded Systems Lab. Responsible for all future digital imaging architectures including parallel ink arrays, dry electro-photographic devices, and image capture systems. Directly responsible for 2.5M LOC and 25M gate SOCs. • Successfully deployed 37 independent product lines within a 6-year period ranging from small business imaging systems to enterprise/industrial copiers, printers, and network scanning machines. • Supervised architectural direction over imaging subsystems with a staff of 36 engineers and scientists. • Institutionalized lab wide agile development methodologies and service orientated architecture principles. This effort resulted in a 2X reduction in software defects and improved time to market by 50%. • Developed system wide process and schedules for new product turn-on from ASIC architecture and co-development through product launch which compressed ASIC turnon schedules by 75% with zero spins. • Development and research work which included: CODEC acceleration through SIMD reinforcement, compiler optimization, voltage and frequency shifting code for efficient power usage for Energy Star certification, hardware acceleration for rendering, and inter-processor communication.
2000-2004	**Engineering Scientist** - Hewlett Packard Co. - Core Technology Laboratories • Acted as team lead and architect for first parallel inline color systems. This was the foundation architecture for the HP LaserJet 4600 (HP's first color inline printer) and all high-speed HP color laser products since. Lead the design of critical areas including: four plane parallel printing, high performance rendering, memory layout structures, and low-level code. • Led a team of six engineers in the delivery of initial board turn-on, new ASIC verification, schedules, requirements, and processor turn-on. Responsible for LaserJet 4600, 5500, and 9500 product delivery.
1995-2000	**Firmware Engineer** - Hewlett Packard Co. – LaserJet Systems Group • Designed a system wide discrete event simulator of LaserJets to explore new architectural concepts. • Directly responsible for the development of: novel image compression technologies, parallel algorithms, memory throughput enhancement (MEt), processor analysis, and compiler efficiencies. • Technical lead for the EPFL university research program for 3 successful projects: DSP/MMX incorporation into the HP graphics engine layer, compiler improvements outside of assembly for MIPS processors, and display list optimizations. Coordinated research work with HP Labs team in Palo Alto and Bristol.
1995-1995	**Software Engineer** - Hewlett Packard Co. - Boise Printer Research • Actively worked with a small team responsible for the delivery of the LaserJet 4j. • Developed a test strategy and test bed for confidence testing of the Windows drivers. • Worked with and mentored Chinese Academy of Science for contractual support of HP drivers.

Education	• **PD EE Columbia University**, New York, NY. 2009 – Degree of Engineer. Research and defense of heterogeneous multi-core SOCs & reconfigurable computing. • **MS CE National Technological University**, Fort Collins, CO. 2001 Concentration on parallel computer architecture and processor interconnections. • **BS CS University of Wisconsin, Milwaukee**. 1994 Minor physics, graduate honors. **University of Washington.** Currently Enrolled - start 2016 Certificate Program on Data Analytics and Deep Learning.

Honorable Mentions

- Mentored intern students (1996 – 2016) – Stanford, Utah State, USC, Steven's Institute, Boise State.
- Member of:
  - Senior Member Institute of Electronic and Electrical Engineers, IEEE Computer Society
  - Senior Member Association of Computing Machinery
  - IEEE Technical Committee on Computer Architecture and Operating Systems
  - Chair and officer of Region 6 IEEE Computer Society: 2001-2003
- Recipient of "Who's Who in Science and Engineering 2006"
- Recipient of Outstanding Engineer Award for USA IEEE Region 6: 2011, 2012, 2013
- HP TechCon 2013 "Let's Make Some Silicon" Chair
- Stanford Graduate School of Business Innovative Leadership Fellow

Patents & Intellectual Property

- Published Patents
  - System and method for controlling print performance 6,977,737
  - A system for high bandwidth imaging across PC chipsets and custom ASICS 7,729,548
  - Page processing and print engine management 7,928,160
  - Print-head assembly Including memory elements 8,882,217
  - Media reproduction device 9,361,852
- Pending Patents
  - •Apparatuses and Methods for Operations Using Compressed and Decompressed Data, •Representing and Edit, •Error Code Calculation on Sensing Circuitry, •Apparatuses and Methods for Data movement, •Providing Auxiliary Services or Functionality on an Apparatus, •Editing an Electronic Document on a Multifunction Peripheral Device, •System and method for processing image data, •Memory management, •Detection of a Security Event, •Data and Instruction Set Encryption, •Printer Interface Selection and Control, •Detecting Signature Lines Within an Electronic Document, •Encryption of Executables in Computational Memory, •Apparatus and Methods for Debugging on a Memory Device
  - >30 other pending patents in-flight

Activities

- Published Work
  - "Extreme Partitioning" IEEE Computer Society Region 6 Seminar
  - Cache Packing and Cache Manipulation. For HP Embedded '99
  - "A method to automatically lock cache lines programmatically", Research Disclosure, June 2004 pp. 823-824
  - "Multicore Load Distribution and Scheduling as a Form of Thermal Balancing", Research Disclosure, May 2009 pp. 505-508
  - "ARM on EFI", HP TechCon 2011
  - "Tile Based Marking, Scaling, and Panning Based on Partial Image Content", hPICS 2011
  - "A System for In-Place On-The-Fly Image Compression and Decompression", TechCon 2012
  - "CDX: A Cycle Accurate and Semi-Cycle Accurate Co-Development System", TechCon 2013
  - "Modular Formatter Architectures", TechCon 2013
  - "A Method for Image Marking Using Data Reflow" hPICS 2014
  - "A Case History of ARM Optimizations" ARM TechCon Invited Speaker 2014, Santa Clara, CA
  - "A Systolic Execution Pipeline for Processing in Memory Devices", Micron DRAM Products Conference, 2015.
  - "Computer Architectural Flops and Futures", IEEE Region 6 Invited Keynote Speaker, May 2016.
  - "Computer Vision as the Killer Application for Processing in Memory", Micron DRAM Products Conference 2016.
  - "Signature Line Detection Scanned Documents", IEEE International Conference on Image Processing, 2016
  - "In Memory Intelligence", IEEE Micro August 2017
  - "IoT for Architects", Packt Publishing, February 2018, London. ISBN 9781788470599